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Electronic and structural properties of the amorphous/crystalline silicon interface

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ABSTRACT

A review of capacitance and conductance measurements on (n) a-Si:H/(p) c-Si structures is presented. Capacitance measurements performed on cells under AM 1.5 illumination at or close to open-circuit voltage are sensitive to the recombination at interfaces, as evidenced by the comparison with photoluminescence results. Capacitance measurements performed in the dark at zero or reverse bias can reveal the presence of interface defects from trapping and release of carriers, but the sensitivity is limited to a few 10^{12} cm^{-2} eV^{-1}. This is partly due to the presence of a strong inversion layer at the c-Si surface. Such a layer has been revealed from coplanar conductance measurements, which allow a precise determination of the conduction band offset, found equal to 0.15 ($\pm$0.04) eV. As shown by spectroscopic ellipsometry, a thin undoped silicon layer deposited under conditions that normally produce polymorphous silicon can be epitaxially grown onto c-Si prior to the (n) a-Si:H layer. Electrical measurements indicate that this additional buffer layer is not detrimental and can slightly improve the interface quality.

1. Introduction

Silicon heterojunction solar cells combining crystalline and thin film silicon technologies are attracting much interest. This is because very high efficiencies (above 22%) have been demonstrated, while, from a technical point of view, the energy consumption and cost effective processing steps used to form the junctions or back surface field in the traditional crystalline solar cell fabrication are replaced with the low temperature processing steps of silicon thin film deposition [1]. Thanks to the use of various characterization techniques some physical aspects of the heterojunction between hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si) have been clarified, and significant improvements in solar cell performance have been obtained in the past few years [2–8]. However, there is still a number of interface related issues that need to be investigated. We here give a summary of characterization results obtained on (n) a-Si:H/(p) c-Si interfaces using a set of both electrical and optical techniques: capacitance and conductance measurements, spectroscopic ellipsometry, and photoluminescence. We emphasize the potentialities and limits of these techniques for the determination of interface parameters such as interface defect densities, capture cross sections, and band offsets. Finally, we address the role of the so-called "intrinsic" buffer layer, and discuss its amorphous or crystalline nature related to possible epitaxial growth.

2. Experimental details

Two types of solar cells based on p-type c-Si were fabricated on flat Czochralski c-Si wafers (<100> oriented, p-type, $\rho = 14$–$22\ \Omega$ cm) and analysed. Single heterojunction solar cells have an aluminium (Al) back surface field, while double heterojunction solar cells have a back interface consisting of a (p) c-Si/(p) a-Si:H heterojunction (Fig. 1). In both types of solar cells, the front emitter consists of an (n) a-Si:H layer deposited by rf PECVD (13.56 MHz) from a silane–phosphine mixture at a pressure of 50 mTorr, power density of 6 mW/cm^2, and substrate temperature of 200 °C. Before the thin-film deposition, the c-Si surface was prepared by removing the native oxide using a wet chemical etching procedure (HF diluted at 5% in DI water). The influence of an additional undoped buffer layer between a-Si:H and c-Si was also studied. This buffer layer was deposited under conditions that normally lead to undoped hydrogenated polymorphous silicon ((i) pm-Si:H) when deposition is made on glass, namely from a silane–hydrogen mixture at a pressure of 1200 mTorr, power density of 23 mW/cm^2, and substrate temperature of 200 °C. We will show in Section 4 that this layer is actually epitaxially grown onto the c-Si substrate.

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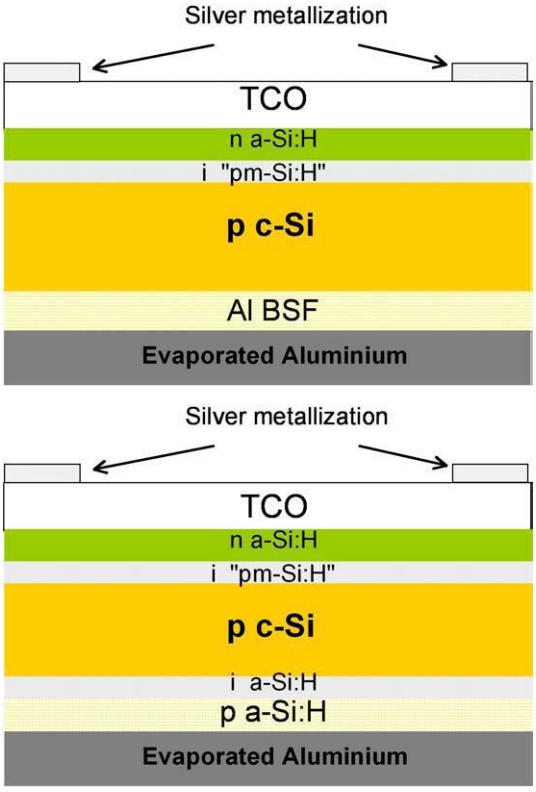

Fig. 1. Schematic view of our single (top) and double (bottom) heterojunction solar cells.

Capacitance measurements were performed on solar cells in two different regimes [9,10], using an HP4284A impedance meter in the frequency range of 100 Hz–1 MHz, with an ac measurement signal of 20 mV. Measurements in the dark at zero bias as a function of frequency and temperature $C(f, T)$ were performed in a cryostat dynamically pumped down to 10^{-5} mbar and in a wide temperature range [100 K–350 K]. Measurements under AM1.5D illumination at forward bias close to the open-circuit voltage, V_{oc}, were performed in air at 300 K.

Photoluminescence measurements were performed on symmetrical wafer structures, for which the thin-film layer sequence of the front side of the cell (emitter stack) was deposited on either side of the c-Si wafer. The samples were excited by a laser diode at a wavelength of 850 nm. The luminescence radiation was detected after dispersion by a monochromator by a liquid-nitrogen cooled InGaAs photodiode. The set-up also allows the measurement of the absolute emitted spectral photon flux density for the determination of the quasi-Fermi level splitting [11].

Conductance measurements were performed on samples consisting of (n) a-Si:H layers fitted with top coplanar Al electrodes [12]. These layers were deposited in the same run on three types of substrates: glass (Corning 1737), Czochralski c-Si wafers (<100> oriented, p-type, $\rho = 14$–$22\ \Omega$ cm), and Float Zone c-Si wafers (<100> oriented, p-type, $\rho = 1$–$5\ \Omega$ cm). Samples with an inserted undoped "pm-Si:H" buffer layer were also fabricated. The thickness of the "pm-Si:H" layer was set at 3 nm, while the thickness of the (n) a-Si:H layer was varied between 20 nm and 200 nm. Since a linear relationship was found between the dc current, I, and dc applied voltage, V, the sample conductance, G, was calculated as the ratio I/V. Measurements were performed in the same conditions as the dark capacitance measurements.

Finally, spectroscopic ellipsometry measurements were performed on these samples to study the growth of the very thin films on crystalline silicon. From these measurements, one can deduce the pseudo-dielectric function $\langle\varepsilon_1\rangle + i\langle\varepsilon_2\rangle$ which is related to the film thickness and optical properties [13]. These data have proved to be efficient in monitoring and controlling the deposition process in a-Si:H/c-Si heterojunctions, in analyzing the layer thicknesses and determining the nature (amorphous or epitaxially grown) of the layer [14,15].

3. Results and discussion

Capacitance data obtained at zero dc bias in the dark are presented in Fig. 2 for single heterojunction solar cells. For the lower quality solar cell (having a conversion efficiency of 12%) with non-optimized front emitter, we observe a capacitance step that is shifted along the temperature axis when the measurement frequency is changed. This is the typical signature of trapping and release processes from defects detected in the so-called space charge spectroscopy [16]. However, such a capacitance step is not observed for the higher quality solar cell (with an efficiency of 16%) obtained after interface optimization. The occurrence of a capacitance step and its dependence with the interface defect density has been analysed in preceding papers [9,17,18]. It has been shown that such a capacitance step is only visible for interface defect densities higher than a few 10^{12} cm^{-2} eV^{-1}. This means that detection of interface defects from the usual space charge spectroscopy technique is much poorer on a-Si:H/c-Si heterojunction solar cells compared to insulator/c-Si interfaces, where values below 10^{10} cm^{-2} eV^{-1} can be detected. This poorer detection limit is related to the peculiar band diagram of the (n) a-Si:H/(p) c-Si interface that is described in Fig. 3. First, it must be stated that in the heterojunction device interface states can exchange either electrons with a-Si:H or holes with c-Si, while in the case of the insulator/c-Si interface exchanges are only possible with c-Si since the insulator cannot provide free carriers. Exchanges of electrons at the interface will add a contribution to the a-Si:H depletion capacitance, which is much higher than the c-Si depletion capacitance. These two capacitances being in series, the sensitivity to the exchange of electrons will be very poor. Exchanges of holes at the interface will add a contribution to the c-Si depletion capacitance, which is indeed directly reflected in the total capacitance. So, only the exchange of holes at the interface can produce a strong capacitance step in the $C(T)$ curve. However, if the density of interface states is low enough that it does not modify the band diagram compared to the ideal band diagram without interface states, it can be seen from Fig. 3 that the strong band bending imposed by the heterojunction produces a strong inversion layer at the c-Si surface. The interface Fermi level is then very close to the conduction

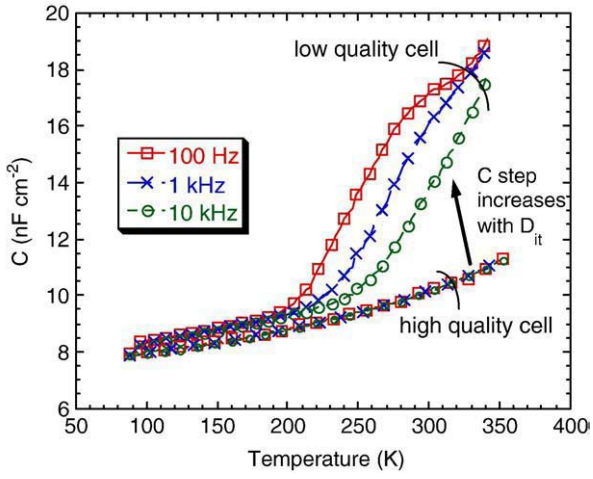

Fig. 2. Zero bias capacitance measured on two solar cells in the dark as a function of temperature at three frequencies. The capacitance step is not visible on the best cell (for which the defect density at the emitter interface, D_{it}, is below 5×10^{12} cm^{-2} eV^{-1}). It increases when D_{it} increases.

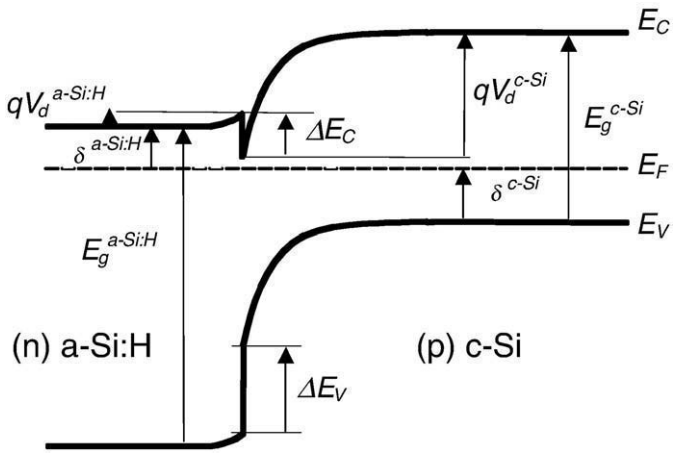

Fig. 3. Equilibrium band diagram of the (n) a-Si:H/(p) c-Si heterojunction for a defect-free interface. The total diffusion potential V_d is the sum of the parts in a-Si:H and c-Si, $V_d^{a\text{-}Si:H}$ and $V_d^{c\text{-}Si}$, respectively; $E_g^{a\text{-}Si:H}$ and $E_g^{c\text{-}Si}$ are the a-Si:H and c-Si band gap energies; $\delta^{c\text{-}Si}$ is the difference between the Fermi level and the valence band maximum in c-Si, while $\delta^{a\text{-}Si:H}$ is the difference between the conduction band mobility edge and the Fermi level in a-Si:H. Also indicated are the conduction and valence band offsets, $\Delta E_C = E_C^{a\text{-}Si:H} - E_C^{c\text{-}Si}$ and $\Delta E_V = E_V^{c\text{-}Si} - E_V^{a\text{-}Si:H}$.

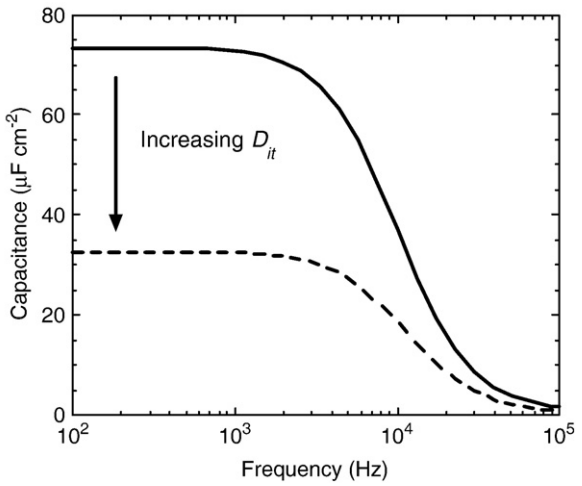

Fig. 4. Example of capacitance versus frequency calculated at 300 K at open-circuit voltage under AM1.5 illumination for a single heterojunction cell for two values of the emitter interface defect density (D_{it}): 10^{10} cm^{-2} eV^{-1} (solid line) and 2×10^{12} cm^{-2} eV^{-1} (dashed line). The low frequency plateau (C_{LF}) decreases when D_{it} increases.

band, and very far from the valence band. The emission of holes is then not possible on the timescale of the experiment in the covered frequency range. Indeed, the exchange of holes due to the ac bias modulation can only occur if the emission frequency of holes e_p is larger than the angular frequency ω. The emission frequency of holes, e_p, is given by

$$e_p = \nu_p \exp\left(-\frac{E_F - E_V}{k_B T}\right), \quad (1)$$

where ν_p is the attempt-to-escape frequency. One can thus calculate the value of $E_F - E_V$ that satisfies $e_p = \omega$ for the highest temperature of 350 K and for the lowest frequency of 100 Hz. The results are given in Table 1 for various values of ν_p. It can be seen that for the highest value of ν_p, the value of $E_F - E_V$ (0.77 eV) is still too low compared to the actual value (>0.85 eV) at the interface when a strong inversion layer exists. Therefore, the response of holes cannot be detected in this frequency and temperature range for low interface defect densities. On the opposite, for high interface defect densities, the band bending can be sufficiently modified (to accommodate charge neutrality) so that the interface Fermi level gets closer to midgap. The response of holes can then be detected in the explored range, and this response will also be larger because the number of exchanged carriers is proportional to the interface density of states.

Since the traditional capacitance space charge spectroscopy has insufficient sensitivity to characterize high quality solar cells, we proposed a few years ago to use capacitance measurements as a function of frequency at forward bias close to or at open-circuit voltage [10]. Under these conditions, a plot of the capacitance versus frequency exhibits a low frequency plateau, C_{LF} [10]. This is a diffusion capacitance, which is related to the diffusion and recombination of free carriers. Thus, it is almost independent of temperature, and, contrary to the trapping-and-release capacitance, measurements can be performed only at room temperature (which is more practical), to obtain a diagnostic of the quality of the interface, just by considering the value of C_{LF} [10,19]. Indeed, C_{LF} mainly reflects the number of free electrons in c-Si that can be modulated by the applied ac bias. Interface states influence C_{LF} because they can act as recombination centres, which decrease the free carrier densities compared to the ideal defect-free interface case. As a consequence, C_{LF} decreases when the interface defect density increases, as can be seen in Fig. 4. This is completely different from the capacitance step measured as a function of temperature in the usual trapping and release regime in the dark at zero dc bias, where the capacitance increases when defect densities increase (as indicated in Fig. 2). Since C_{LF} is sensitive to the recombination at interface states, it depends on the defect capture cross sections and on the band offset. We have recently shown that a plot of C_{LF} versus the recombination rate at interface states yields a unique curve, while the

Table 1
Position of the Fermi level at the interface that satisfies $e_p = \omega$ for the highest temperature of 350 K and for the lowest frequency of 100 Hz used in the measurements, for three values of the attempt-to-escape frequency.

ν_p (s^{-1})	10^{10}	10^{12}	10^{14}
E_F–E_V (eV)	0.50	0.64	0.77

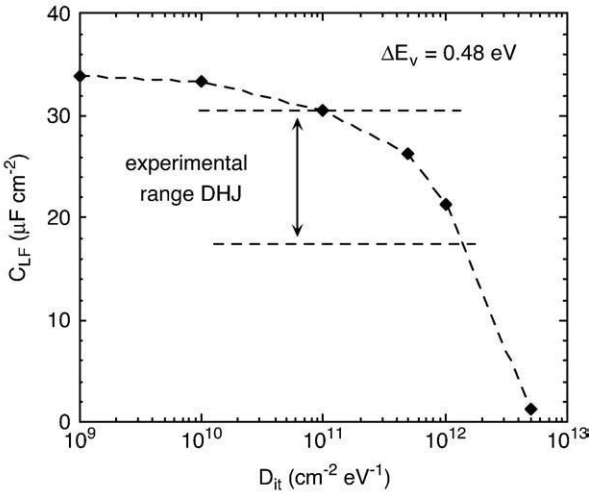

Fig. 5. Calculated low frequency capacitance (at open-circuit voltage under AM1.5 illumination) of a double heterojunction (DHJ) solar cell as a function of interface states density at the back interface. The valence band offset was set at 0.48 eV. The interface defect density at the front interface was fixed at 10^{12} cm^{-2} eV^{-1} and the conduction band offset was set at 0.2 eV. The range of experimental data gathered from measurements performed on our DHJ solar cells is also indicated.

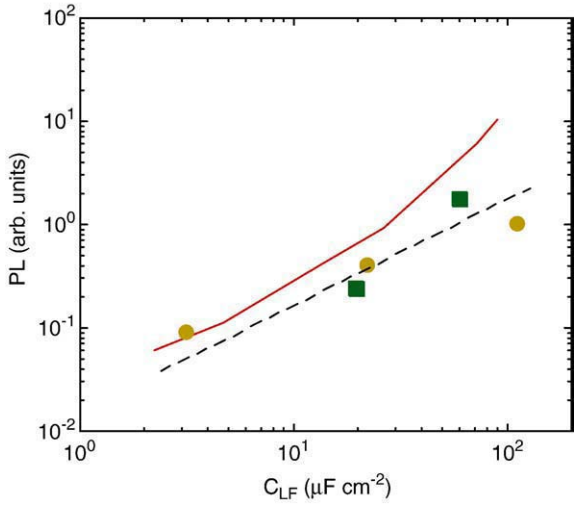

Fig. 6. Integrated band-to-band recombination photoluminescence signal (*PL*) versus low frequency capacitance (C_{LF}) for SHJ (squares) and DHJ (circles) cells. The calculated dependence assuming a back surface recombination velocity of minority carriers equal to 10^2 cm/s and varying the front interface defect density is shown in plain line. The dashed line indicates a linear dependence of *PL* on C_{LF}.

same value of interface recombination rate can be obtained for different values of capture cross sections, defect densities and conduction band offset [19].

Moreover, C_{LF} being intimately linked to the free carrier concentrations, it is sensitive to the recombination, wherever it occurs. In particular it is sensitive also to the back interface parameters. To illustrate this fact, we performed calculations of C_{LF} in a double heterojunction solar cell, where the back surface field is provided by a back (p) c-Si/(p) a-Si:H interface. We fixed the front interface parameters, and only varied the back interface parameters. Results are shown in Fig. 5. As expected, C_{LF} decreases with the back interface density, and also depends on the valence band discontinuity [10].

A further illustration of the sensitivity of C_{LF} to recombination is provided by the comparison with the band-to-band recombination photoluminescence (*PL*) signal. At a given temperature, the *PL* signal is to a first degree proportional to the product of free electron and hole densities (integrated over the whole c-Si volume) [20]. Recombination at interfaces produces a decrease of these densities, and thus of the *PL* signal. Numerical calculation of both *PL* and C_{LF} was performed in an SHJ structure, where the front interface defect density was varied. As shown in Fig. 6, it was found that *PL* and C_{LF} are theoretically well correlated. They both increase with interface quality due to the lower recombination. Experimental data obtained on both SHJ and DHJ solar cells are also given in the figure. They follow the trend predicted by our theoretical analysis. A detailed discussion on the comparison between C_{LF} and *PL* can be found elsewhere [21].

So far, we mainly discussed capacitance measurements in two different regimes. The lack of sensitivity of the usual trapping and release regime was mainly attributed to the peculiar band bending at the (n) a-Si:H/(p) c-Si interface, and in particular to the strong band bending related to the band offsets between both materials. We already provided some hints at the existence of a strong inversion layer from the bias dependence of the dark capacitance under reverse bias [22]. With the help of numerical calculations, we proved that the presence of a strong inversion layer can induce large errors in the determination of the conduction band offset from the *C–V* method [19]. We here want to emphasize other experimental results that indicate the presence of this strong inversion layer. These results are obtained from very simple coplanar conductance measurements [12], performed on samples where the (n) a-Si:H layer was deposited in the same run on both glass and (p) c-Si substrates. In both kinds of structures, an activated behaviour was observed [12],

$$G = G_0 \exp\left[-E_G / (k_B T)\right], \tag{2}$$

k_B being Boltzmann's constant, T the temperature, G_0 the prefactor and E_G the activation energy. As summarized in Table 2, the conductance measured with coplanar electrodes deposited on top of the (n) a-Si:H layer is several orders of magnitude higher when the a-Si:H layer is deposited onto (p) c-Si than onto glass. For the glass samples, the activation energy ($\approx$0.2 eV) is typical of (n) a-Si:H, while a much lower value (<0.02 eV) was found on the c-Si samples. In addition, when the a-Si:H layer is etched, thus leaving a free c-Si surface between the electrodes, the conductance decreases by several orders of magnitude and the activation energy increases to 0.72 eV [12], which is then related to the conduction process through the (n) a-Si:H/(p) c-Si diode. Thus, the high coplanar conductance with low activation energy measured on (n) a-Si:H/(p) c-Si samples comes from the interface, due to the strong inversion layer where a high electron current can flow along the interface. One can easily understand that this channel conductance is strongly dependent on the Fermi level position at the interface, which is in turn strongly dependent on the conduction band mismatch between (n) a-Si:H and (p) c-Si, as shown in Fig. 7. The conductance is related to the sheet electron density, defined as the integral of the electron concentration over the c-Si wafer, d,

$$N_s = \int_0^d n(x)dx \tag{3}$$

through $N_s = L\,G/(q\,\mu_n\,h)$, where h is the width of the electrodes, L the gap between them, and μ_n is the electron mobility in the inversion layer. Using AFORS-HET [23], we calculated the free carrier profile for various values of the conduction band offset, $\Delta E_C = E_C^{\text{a-Si:H}} - E_C^{\text{c-Si}}$. N_s was then computed and was found to also exhibit an activated behaviour, $N_s = N_{s0} \exp\left[-E_a/(k_B T)\right]$. As seen in Fig. 7, the activation energy of N_s, E_a, is not equal to $E_C - E_F$ at the interface (which slightly depends on T), but it follows the same trend with ΔE_C. The experimental values of E_G of Table 2 can then be compared to E_a in order to determine ΔE_C. For a proper determination, one should take into account the temperature dependence of μ_n, which is weak and can be expressed as a power-law dependence, $\mu_n \sim T^{-\alpha}$, with $0 \le \alpha \le 2.4$ [19]. With these precautions, and from measurements performed on several series of samples, we found $\Delta E_C = 0.15 \pm 0.04$ eV [24]. To our knowledge, this is the most straightforward and most precise determination of this parameter, that is very important for the device simulation of solar cells, and it is in good agreement with recent work from photoyield spectroscopy [5,7] that is rather sensitive to the valence band offset.

Table 2
Parameters of samples used to study the effect of an undoped buffer layer deposited under conditions that normally lead to pm-Si:H on glass: thickness of this (i) "pm-Si:H" layer ($d_{\text{pm-Si:H}}$), thickness of the (n+) a-Si:H layer ($d_{\text{a-Si:H}}$), value at 300 K (G) and activation energy (E_G) of the coplanar conductance for samples.

Sample characteristics			Glass substrate		CZ c-Si substrate		FZ c-Si substrate	
Number	$d_{\text{pm-Si:H}}$ (nm)	$d_{\text{a-Si:H}}$ (nm)	G (S)	E_G (eV)	G (S)	E_G (eV)	G (S)	E_G (eV)
604122	0	20	1.5×10^{-9}	0.26	6.6×10^{-4}	0.018	5.7×10^{-4}	0.017
604125	3	20	8.0×10^{-9}	0.28	1.4×10^{-3}	0.015	1.8×10^{-3}	0.015
604123	0	100	8.0×10^{-7}	0.17	8.6×10^{-4}	0.018	6.0×10^{-4}	0.018
604126	3	100	8.5×10^{-7}	0.17	1.5×10^{-3}	0.016	2.0×10^{-3}	0.016
604124	0	200	1.4×10^{-6}	0.17	8.0×10^{-4}	0.019	6.6×10^{-4}	0.017
604127	3	200	2.0×10^{-6}	0.16	1.4×10^{-3}	0.016	1.8×10^{-3}	0.015

Deposition and measurements were performed on three types of substrates: glass, (p) Cz c-Si (14–22 Ω cm) and (p) FZ c-Si (1–5 Ω cm), both c-Si wafers being flat and (100) oriented.

We finally turn to the discussion of the influence of a thin undoped layer (called intrinsic layer [1], although this denomination is not correct in the usual sense of semiconductor physics) inserted between the (p) c-Si and (n) a-Si:H. It should be noted that there is a controversy on the need of such a layer. Some authors claim that it is beneficial [3], while others get good results without it and do not see significant improvements if they introduce it [5]. One reasonable explanation for the benefit of this undoped buffer layer is that the density of states in undoped a-Si:H is weaker than in doped a-Si:H, so we can expect to have less interface defects when the heterointerface is formed with undoped rather than doped a-Si:H. We have shown in previous works that undoped hydrogenated polymorphous silicon has a lower defect density than usual undoped a-Si:H [25]. This is why we investigated the effect of an undoped layer deposited under plasma conditions that normally produce pm-Si:H when the deposition is done on a glass substrate. Here the undoped layer is deposited onto the c-Si wafer prior to the (n) a-Si:H deposition. The c-Si samples were the same as for the solar cells, as described in the Experimental detail section. In particular, we recall here that the wafers were (100) oriented. Sets of samples with or without a 3 nm thick undoped "pm-Si:H" were thus fabricated (see Table 2). Spectroscopic ellipsometry measurements were systematically performed on all samples. As can be seen in Fig. 8a the spectra obtained for #604122 (20 nm a-Si:H) and #604125 (3 nm pm-Si:H + 20 nm a-Si:H) are very different from that of the reference c-Si alone (after usual HF treatment of the surface). We do not see any difference in the spectra obtained on samples deposited onto c-Si. This means that this "pm-Si:H" layer is behaving here just like c-Si, suggesting that there is an epitaxial growth of silicon in these conditions. To validate this suggestion, a set of additional samples was fabricated, consisting of a layer deposited under pm-Si:H conditions with various thickness (3, 6, and 12 nm) followed by a 10 nm thick a-Si:H layer. In addition, a 20 nm thick pm-Si:H layer was deposited on the same substrate without any a-Si:H. The comparison of the $\langle\varepsilon_2\rangle$ spectra is shown in Fig. 8b. Obviously, the signal measured on the sample with only the 20 nm "pm-Si:H" layer is very close to that of the reference c-Si sample. In addition, when the a-Si:H layer is deposited on top of the "pm-Si:H", there is almost no influence of the thickness of the "pm-Si:H" layer. This is a further proof that the layer deposited under pm-Si:H conditions leads to epitaxial growth onto the c-Si wafer. This also confirms some previous HRTEM data, where a crystalline nature could be identified in the region where "pm-Si:H" was deposited [26]. Finally, the important question for solar cells is whether such an undoped "pm-Si:H" layer is beneficial or not. Concerning the solar cell performance, our best results for (n) a-Si:H/(p) c-Si solar cells (efficiency close to 17% with an open-circuit voltage of 650 mV) have been obtained so far with such a "pm-Si:H" layer [27]. The effect on the coplanar conductance has also been analysed. As can be seen in Table 2, a slight but systematic increase of the conductance and decrease of its activation energy has been observed when the additional undoped "pm-Si:H" layer is present. This reveals a slightly stronger band bending at the interface, which is beneficial in terms of recombination at the interface since the front surface field is enhanced. Thus, from our results, a thin epitaxially grown undoped silicon layer, obtained from silicon deposition conditions that normally lead to a pm-Si:H layer when deposition is performed on glass, is beneficial for solar cell performance. However, one should avoid to extrapolate this conclusion to any epitaxially grown layer. Other authors recently concluded that epitaxial growth of a buffer layer can degrade the solar cell performance [28]. We would like to stress that the information on epitaxial growth coming from spectroscopic ellipsometry (or from other structural characterization like TEM) is

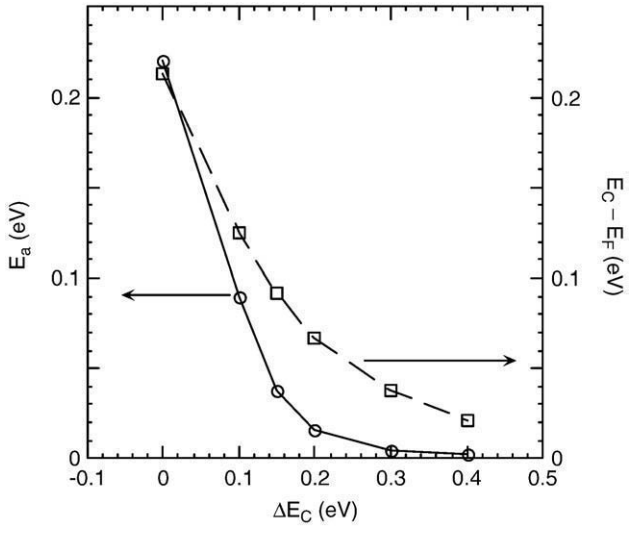

Fig. 7. Activation energy of the sheet electron density, E_a, and of the position of the Fermi level relative to the c-Si conduction band at the (n) a-Si:H/(p) c-Si interface at 300 K, $E_C - E_F$, calculated as a function of the conduction band offset. All calculations were performed with a doping density in c-Si, $N_a = 7 \times 10^{14}$ cm^{-3}.

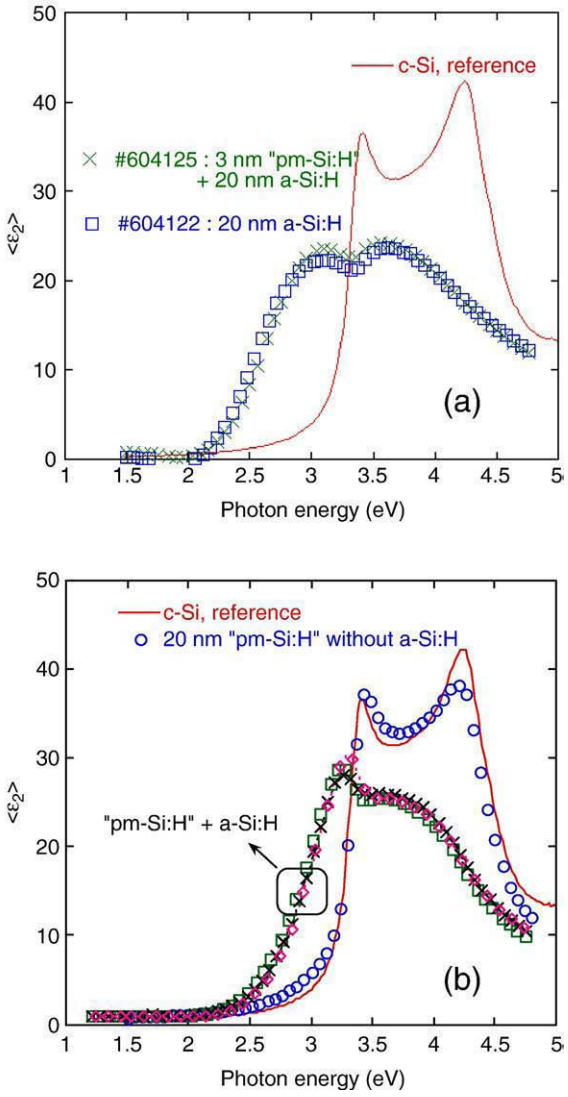

Fig. 8. Imaginary part of the pseudo-dielectric function. In (a) are compared the spectra of samples #604122 and #604125 deposited onto CZ c-Si; a reference spectrum measured on the c-Si alone is also shown for comparison. In (b) we compare the spectra of 4 additional samples on the same c-Si substrate: a 20 nm thick layer deposited under pm-Si:H conditions (o), and three samples where a 10 nm thick a-Si:H layer was deposited on top of a "pm-Si:H" layer, 3 nm (□), 6 nm (×), and 12 nm (◇) thick.

sensitive to defect densities of the order of the percent of the silicon atom density. This is much higher than the amount of electronic defects that can lead to a very poor electronic interface quality. Therefore, two interfaces that appear equal from the structural point of view can have very different electronic properties and structural characterization needs to be completed with electronic characterization. In other words, one can produce epitaxial layers that contain either a high or a low defect density from the electronic point of view, while these layers cannot be distinguished from ellipsometry data. Our combined ellipsometry and electronic measurements indicate that a "pm-Si:H" layer deposited onto c-Si, which actually is an epitaxially grown c-Si layer, is a high electronic quality layer, which should contain a low defect concentration.

4. Conclusion

We have used various characterization techniques to gain insight into the physics of interfaces in silicon heterojunction solar cells. The difference in the physical mechanisms responsible for the capacitance measured in the dark at zero bias and at open-circuit voltage under illumination has been emphasized. The former is determined by trapping and release of carriers at interface defects, but it has a limited sensitivity to interface defects due to the peculiar band bending at the a-Si:H/c-Si interface. The latter is strongly influenced by the recombination of free carriers, and it is therefore sensitive to both interfaces, at the front emitter and at the back surface. This has been correlated to photoluminescence measurements. One very simple and very powerful technique is the coplanar conductance measurement. This allowed us to determine the conduction band offset with a good precision. It has also been used to investigate the effect of a thin undoped layer deposited under conditions that lead to pm-Si:H on glass. Spectroscopic ellipsometry indicate that this layer is epitaxially grown on the silicon wafer. Contrary to some reports in the literature, the solar cell performance is not deteriorated (it is even slightly improved) by the presence of this epitaxially grown layer, suggesting that such a "pm-Si:H" layer contains a low quantity of recombination centers. Conductance measurements suggest a slightly more pronounced band bending at the (n) a-Si:H interface, which is also beneficial for the solar cell performance.

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