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Study of the interfacial properties of amorphous silicon/n-type crystalline silicon heterojunction through static planar conductance measurements

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We have previously shown from static planar conductance measurements that a strong inversion layer does exist in c-Si at the (n) a-Si:H/ (p) c-Si interface. This allowed us to determine the conduction band offset with a good precision (ΔE_C = 0.15 +/- 0.04 eV). The same technique is now applied to study (p) a-Si:H/ (n) c-Si interfaces. We demonstrate that a strong inversion layer (of holes) also exists at the c-Si surface of this hetero-interface. Analysis of our planar conductance data with the help of numerical simulations allows us to set a lower limit to the valence band offset, $\Delta E_V = E_{V,a\text{-}Si:H} - E_{V,\,c\text{-}Si}$: $\Delta E_V > 0.28$ eV.

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1 Introduction Thin-films heterojunctions solar cells combining hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si) have demonstrated efficiencies up to 23% [1]. Another interest in this technology is the low temperature at which the junction is processed (T<250°C) reducing the costs in comparison with the conventional high temperature diffused homojunctions.

Since the crystalline substrate is high quality silicon, and the amorphous layer is very thin, the performance of these structures is mainly determined by the band offset and the amount of defects at the interface [2].

Planar conductance measurement as a function of temperature is a powerful tool to study this interface and the method highlighted the existence of a strong electron inversion layer at the c-Si surface of (n) a-Si:H/(p) c-Si heterojunctions, from which we determined the conductance band offset with a very good precision: ΔE_C = 0.15 +/- 0.04 eV [3, 4].

Preliminar planar conductance measurements applied to the symmetric structure, between p-type a-Si:H and n-type c-Si, suggested the presence of a strong hole inversion layer at this interface [5]. Here, we explore the temperature dependence of the conductance on various samples and focus on the existence of this hole inversion layer and on the potential determination of the valence band offset, ΔE_V.

2 Samples and experiment We studied two series of boron doped a-Si:H films with various thicknesses (15 nm, 60 nm, 120 nm) deposited in a standard radio-frequency (13.56 MHz) Plasma Enhanced Chemical Vapor Deposition (PECVD) reactor on two kinds of substrates: Float Zone, n-type c-Si wafers (<100> oriented, ρ = 1-5 Ω cm, W = 300 µm) and Corning glass (1737) substrates.

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The films were deposited from a silane (SiH_4) and dopant gas mixture. The main differences between the two series was that the doping gas was diborane (B_2H_6) and the temperature of deposition was taken at 140 °C in the first one, while trimethylboron (TMB) and a deposition temperature of 200 °C were used in the second one.

Table 1 Parameters of the samples as deposited: $d_{a\text{-}Si:H}$: thickness of the (p) a-Si:H layer; T_{dep}: temperature of deposition; G_{glass}: planar conductance at 300 K on glass; $G_{c\text{-}Si}$: planar conductance at 300 K on (n) c-Si; $E_{a\ glass}$: activation energy of the conductance on glass (determined above 300 K); $E_{a\ c\text{-}Si}$: activation energy of the conductance on (n) c-Si.

Sample	$d_{a\text{-}Si:H}$ (nm)	T_{dep} (°C)	Doping gas	G_{glass} (S)	$G_{c\text{-}Si}$ (S)	$E_{a\ glass}$ (eV)	$E_{a\ c\text{-}Si}$ (eV)
9012903	15	140	B_2H_6	-	1.56×10^{-4}	-	0.017
9012904	60	140	B_2H_6	-	2.05×10^{-4}	-	0.033
9012905	120	140	B_2H_6	-	1.57×10^{-4}	-	0.025
903242	60	200	TMB	3.44×10^{-10}	1.61×10^{-4}	0.36	0.041
903243	120	200	TMB	3.82×10^{-10}	1.48×10^{-4}	0.36	0.042

Finally, 300 nm thick parallel Aluminum coplanar electrodes were evaporated on the front side of the samples. Table 1 summarizes the studied sample properties. The dark current was measured for voltages in the range [-5 V; +5 V] in a cryostat chamber pumped down to 10^{-5} mbar. The temperature was changed between 123 K and an upper limit T_{max} which was changed from 303 K to 423 K, 473 K and 523 K, in order to check for the effect of annealing.

3 Results The most striking feature is that the planar conductance measured for (p) a-Si:H deposited on (n) c-Si wafer is several orders of magnitude higher than the one measured for samples deposited on glass substrates, as can be seen in Fig. 1.

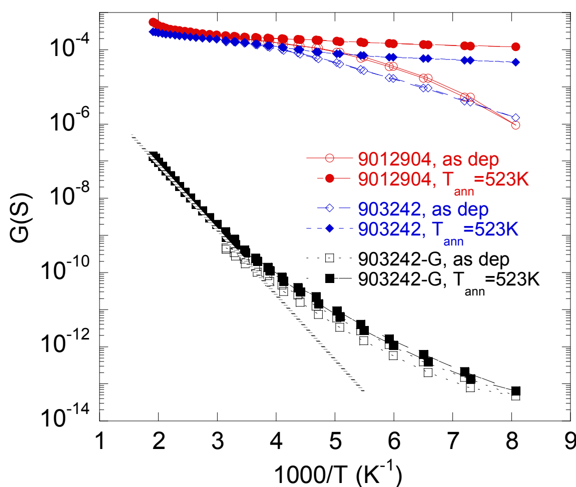

Figure 1 Arrhenius plot of the planar conductance measured in the dark for the samples with a 60nm thick layer of (p) hydrogenated amorphous silicon deposited on glass and c-Si substrate before annealing (open symbols) and after annealing at 523 K (full symbols).

For the glass samples, the range of conductance is compatible with conductivities that are typical of (p) a-Si:H. At low temperatures, there is a pronounced curvature in the Arrhenius plot. If the conductance (or conductivity) is plotted against $T^{1/4}$, the curve tends to become linear, suggesting that hopping might become dominant at low T [6]. Therefore, activation energies of the conductance were deduced on the glass samples only from data above room temperature. Annealing at temperatures above the deposition temperature resulted in a slight increase of the conductance.

For the c-Si samples, we observed a stronger decrease of the conductance with decreasing temperature below 200 K. This stronger decrease disappeared when the samples were annealed at 473 K and 523 K.

In order to verify that the high conductance measured on c-Si samples is not due to the bulk c-Si, sample 903242 was etched using a reactive ion etching system with SF_6/O_2 mixture. This treatment operates perpendicularly to the sample, removing the a-Si:H layer except where it is masked by the top metallic electrodes. After etching, the conductance dramatically decreased, as can be seen in Fig. 2.

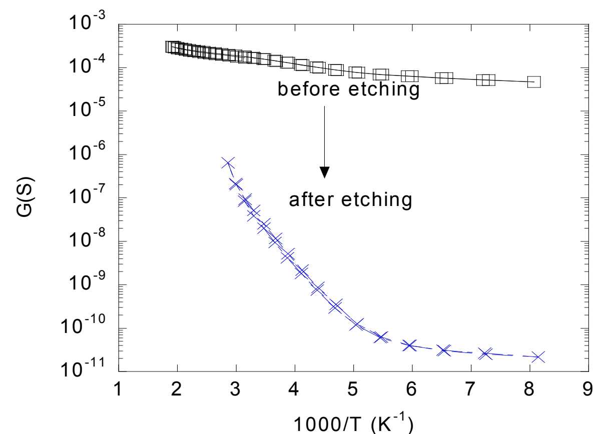

Figure 2 Arrhenius plot of the planar conductance measured in the dark for the sample 903242 on crystalline silicon before and after etching.

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4 Discussion Figure 3 represents a simplified equivalent electrical circuit for the current transport in the (p) a-Si:H/(n) c-Si structure. It highlights three possible paths for the carriers that will contribute to the planar conductance.

The first one is the path in the amorphous layer only. This can be neglected since measurements performed on glass samples indicate a very low conductance compared to that of the c-Si samples. Regarding the second path, the conductance of the (n) c-Si wafer is indeed orders of magnitude higher than the conductance of the (p) a-Si:H layer. However, its contribution to the planar conductance is also negligible. This is because whatever the sign of the polarization, there is a reverse biased diode limiting the current flowing through this path between the two top coplanar electrodes. We can thus conclude that the high conductance measured on the c-Si samples is due to the third path. This path does exist due to the presence of a 2D hole inversion layer at the interface. Figure 4 illustrates the corresponding band diagram. An experimental proof for this path being dominant when a-Si:H is deposited on top of the c-Si is provided by the comparison of measurements on the c-Si sample before and after etching of the a-Si:H layer (Fig. 2). The drastic decrease of conductance after etching is explained by the suppression of the strong inversion layer of holes, the conductance after etching being then determined by the sum of the contributions coming from the second path and by from a remaining surface path (which depends on the surface condition after etching and is not monitored).

Actually, a more refined equivalent circuit should take into account the vertical access resistances between the electrodes and the hole inversion layer, which are caused by the vertical conduction through the a-Si:H layer and the vertical flow of holes across the interface, both being thermally activated. This can be the explanation for the conductance decrease observed in the c-Si samples at low temperatures, where these access resistances might become non negligible. Annealing at temperatures above 473 K might decrease these access resistances significantly due to a better activation of dopants in a-Si:H and changes at the interface that favour the flow of holes accross it.

We introduced a density of gap states in a-Si:H consisting of two exponential bandtails and two Gaussian distributions of monovalent states that have been chosen so to be representative of dangling bond defects in agreement with the defect pool model [8]. These along with the net doping density were adjusted to reproduce the temperature dependence of the (p) a-Si:H conductivity, as can be seen in Fig. 5. Only the dependence at high temperature is well reproduced since no hopping transport is taken into account in AFORS-HET. The band gap of a-Si:H was here taken at $E_g^{c\text{-}Si}$ = 1.75 eV, and the position of the Fermi level was found equal to 0.38 eV, which is a reasonable value for p-type a-Si:H.

Numerical simulations have been performed with the AFORS-HET software [7] in order to determine the impact of the hole inversion layer on the conductance.

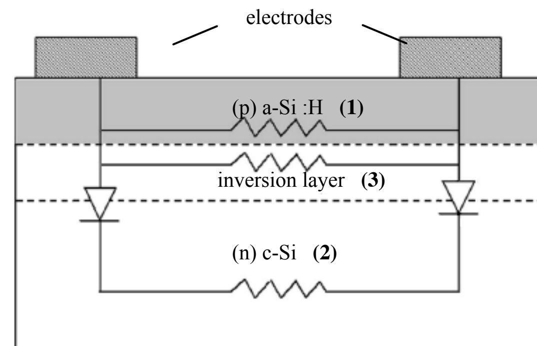

Figure 3 Simplified equivalent electrical circuit showing the contributions for the global conductance.

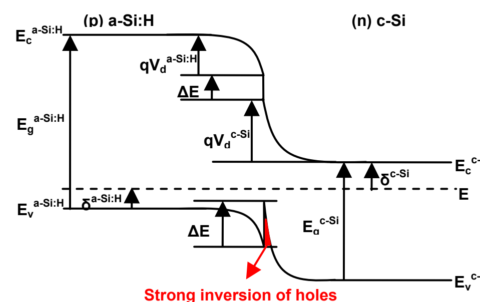

Figure 4 Band diagram of the (p) a-Si:H/ (n) c-Si heterojunction emphasizing the strong inversion layer of holes at the c-Si surface.

Finally, after having fixed the a-Si:H parameters, we combined the a-Si:H layer with an n-type c-Si substrate ($N_a = 2\times10^{15}$ cm^{-3}) to simulate the (n) a-Si:H/ (p) c-Si heterojunction.

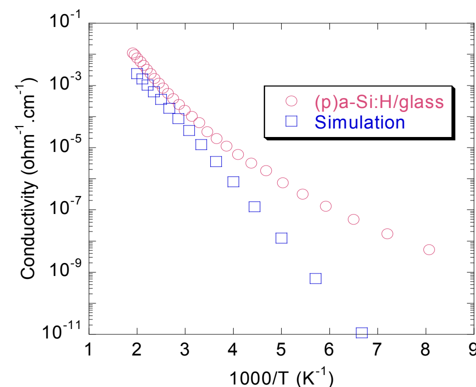

Figure 5 Arrhenius plot of the planar conductance measured in the dark for the sample 903242 on glass substrate compared to simulation. Hopping is not taken into account in the simulation, which can explain the disagreement at low temperatures.

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If the planar conductance is determined by the third path in Fig. 3, as discussed before, the conductance can be written

$$G_{\text{int}} = q\mu_p P_s h / L \tag{1}$$

where q is the electron charge, μ_p the mobility of holes, h and L the length of the parallel electrodes and the distance between them, respectively, and P_S is the hole surface density in c-Si obtained by integrating the hole concentration $p(x)$ over the c-Si wafer thickness $d_{c\text{-}Si}$,

$$P_S = \int_0^{d_{c-Si}} p(x)dx \tag{2}$$

P_S was calculated for various values of the valence band offset: $\Delta E_v = E_v^{c\text{-}Si} - E_v^{a\text{-}Si:H}$ in order to check the influence of this fundamental parameter and to compare with our experimental results. To obtain P_S from experimental conductance data, the hole mobility is the only parameter in Eq. (1) that we do not know exactly, since mobility values in an inversion layer can be significantly lower than in bulk c-Si [9], with a lower temperature dependence. The experimental temperature dependence of P_s was determined from conductance measurements of samples 903242 and 9012903 using two limiting cases for the hole mobility values: $\mu_p(\text{T}) = \mu_{300} \times (\text{T}/300)^{-2.2}$ cm^2 V^{-1} s^{-1}, which is relevant for bulk c-Si [10], and a lower limit temperature independent value, $\mu_p = 160$ cm^2 V^{-1} s^{-1}. Results are depicted in Fig. 6.

Globally, experimental and simulated data fall in the same range except when ΔE_v is too low. This is because a too low valence band offset implies that the hole inversion layer is too weak to account for the higher experimental P_s values. This allows us to put a lower limit of 0.28 eV for ΔE_v, $\Delta E_v > 0.28$ eV. Note that this lower boundary is compatible with the value $\Delta E_v = 0.46 \pm 0.05$ eV that had been obtained by other authors from another experimental technique [11].

In the present simulations no interface defects were introduced. In high quality interfaces required for solar cells the amount of these defects should be low enough so that they have negligible effect on the band bending and thus on the planar conductance. However, new simulations are needed to verify it. Also, the temperature dependence of bandgap energies has to be introduced in the simulations. This will not change the lower boundary value found for ΔE_v but it should allow us to also fix an upper boundary value.

5 Conclusion The comparison of planar conductance measurements of (p) a-Si:H layers deposited on (n) c-Si and glass substrates demonstrates that a strong inversion layer does exist at the (p) a-Si:H/ (n) c-Si interface. Analysis of the data together with numerical modelling allows us to set a lower limit value for the valence band offset, $\Delta E_v > 0.28$ eV. Further work is under way to refine the determination of ΔE_v.

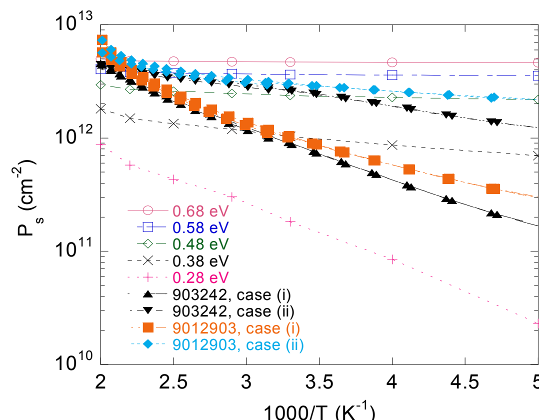

Figure 6 Temperature dependences of sheet hole density in (n) c-Si calculated for different values of ΔE_v; full symbols show results obtained from the conductance measurements for two extreme cases of temperature dependence of the hole mobility, $\mu_p = \mu_{300K} \times (\text{T}/300)^{-\alpha}$; in case (i), μ_{300K}=480 cm^2 V^{-1} s^{-1} and α=2.2, while in case (ii) μ_{300K}=160 cm^2 V^{-1} s^{-1} and α=0.

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